Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented): A method for selectively switching capacitors in a SAR capacitor array that have a common plate thereof interfaced to the input of a comparator, comprising the steps of:

initiating a SAR compare cycle;

switching the other plates the capacitors to be disposed at either a first capacitor reference voltage or a second capacitor reference voltage in a combination and sequence of switching operations defined by a successive approximation search algorithm;

each switching operation in the sequence requiring, after the step of switching, a comparison of the voltage input to the comparator with a compare reference voltage after a predetermined settling time from the time the capacitor combination for the switching operation has been switched; and

controlling the duration of the settling time for each of the switching operations in the sequence such that at least two of the durations are different.

2. (Previously Presented): The method of Claim 1, wherein the first of the switching operations in the sequence is associated with a most significant bit (MSB) in the sequence, which associated first switching operation has a longer duration than at least one of the other switching operations in the associated SAR conversion cycle.

3. (Previously Presented): The method of Claim 2, wherein the second switching operation in the sequence is associated with a second MSB that immediately follows the first switching operation and the second switching operation has a duration substantially equal to that of the first switching operation.

4.(Previously Presented): The method of Claim 2, wherein the SAR capacitor array has a plurality of capacitors associated therewith of different sizes and the one of the capacitors associated with the first switching operation is the largest capacitor in the SAR capacitor array.

5. (Previously Presented): The method of Claim 2, wherein the last of the switching operations in the sequence has the shortest duration.

6. (Previously Presented): The method of Claim 1, wherein the second capacitor reference voltage comprises system ground.

7.(Previously Presented): The method of Claim 1, wherein the step of initiating a SAR conversion cycle comprises impressing an input voltage to be converted to a digital value in the SAR conversion cycle across all of the capacitors in the SAR capacitor array during a tracking phase prior to the first switching operation in the sequence.

8.(Previously Presented): The method of Claim 7, wherein the step of switching the other plate of the capacitors between the first capacitor reference voltage and the second capacitor reference voltage comprises disposing one plate of a select one or ones of the plurality of capacitors to a potential equal to the first capacitor reference voltage and disposing the other plate of each of the remaining capacitors in the SAR capacitor array to a potential equal to the second capacitor reference voltage in accordance with the successive approximation search algorithm.

9.(Previously Presented): The method of Claim 1, wherein the step of controlling the duration of settling time for each switching operation comprises generating a clock with unequal cycles wherein at least one cycle in a clock sequence has a longer cycle than the remaining clock cycles in the clock cycle sequence.

10. (Previously Presented): The method of Claim 9, wherein at least two clock cycles have a longer duration than the remaining clock cycles in the sequence.

11. (Previously Presented): The method of Claim 10, wherein the at least two clock cycles have a substantially similar duration

12. (Currently Amended): A SAR switching control for selectively switching capacitors in a SAR capacitor array that have a common plate thereof interfaced to the input of a comparator, comprising:

a plurality of switches associated with the other plates of each of the capacitors;

a tracking controller for initiating a SAR compare cycle;

a switch controller for controlling said switches to switch the other plates of the capacitors to either a first capacitor reference voltage or a second capacitor reference voltage in a combination and sequence of switching operations defined by a successive approximation search algorithm, the combination associated with a digital value for the capacitors connected to the first capacitor reference voltage;

a latch for latching the output value of the comparator at the end of a comparison cycle wherein each switching operation in the sequence requiring, after switching by said switch controller, a comparison of the voltage input to the comparator with a compare reference voltage after a predetermined settling time, constituting the end of the comparison cycle, from the time the capacitor combination for the switching operation has been switched; and

a clock controller for controlling the duration of the settling time for each of the switching operations in the sequence such that at least two of the durations are different.

13.(Previously Presented): The switch controller of Claim 12, wherein the first of the switching operations in the sequence is associated with a most significant bit (MSB) in the sequence, which associated first switching operation has a longer duration than at least one of the other switching operations in the associated SAR conversion cycle.

14.(Previously Presented): The switch controller of Claim 13, wherein the second switching operation in the sequence is associated with a second MSB that immediately follows the first switching operation and the second switching operation has a duration substantially equal to that of the first switching operation.

15.(Previously Presented): The switch controller of Claim 13, wherein the SAR capacitor array has a plurality of capacitors associated therewith of different sizes and the one of the capacitors associated with the first switching operation is the largest capacitor in the SAR capacitor array.

16.(Previously Presented): The switch controller of Claim 15, wherein the last of the switching operations in the sequence has the shortest duration.

17. (Previously Presented): The switch controller of Claim 12, wherein the second capacitor reference voltage comprises system ground.

18. (Previously Presented): The switch controller of Claim 12, wherein said SAR controller is operable to impress an input voltage to be converted to a digital value in the SAR conversion cycle across all of the capacitors in the SAR capacitor array during a tracking phase prior to the first switching operation in the sequence.

19. (Currently Amended): The switch controller of Claim 18, wherein said switch controller is operable to dispose the other plate of a select one or ones of the plurality of capacitors to a potential equal to the first capacitor reference voltage and dispose the other plate of each of the remaining capacitors in the SAR capacitor array to a potential equal to the second capacitor reference voltage in accordance with the successive approximation search algorithm.

20. (Previously Presented): The switch controller of Claim 12, wherein said clock controller comprises a clock with unequal cycles wherein at least one cycle in a clock sequence has a longer cycle than the remaining clock cycles in the clock cycle sequence.

21. (Previously Presented): The switch controller of Claim 20, wherein at least two clock cycles have a longer duration than the remaining clock cycles in the sequence.

22. (Currently Amended): The switch controller of Claim 21, wherein the at least two clock cycles have a substantially similar duration.